UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

ACER, INC., ACER AMERICA CORPORATION and GATEWAY, INC., Plaintiffs, v. TECHNOLOGY PROPERTIES LTD., PATRIOT SCIENTIFIC CORPORATION, ALLIACENSE LTD., Defendants.	Case No. 5:08-cv-00877 PSG **(Re: Docket Nos. 356, 357, 358, 374)**
HTC CORPORATION, HTC AMERICA, INC., Plaintiffs, v. TECHNOLOGY PROPERTIES LTD., PATRIOT SCIENTIFIC CORPORATION, ALLIACENSE LTD., Defendants.	Case No. 5:08-cv-00882 PSG **(Re: Docket Nos. 385, 387, 388, 403)**

CLAIM CONSTRUCTION ORDER

On November 30, 2012, following reassignment of this case to the undersigned with the consent of the parties and in light of the retirement of Chief Judge Ware, and the completion of an

extended *Markman* hearing, the court issued an order from the bench construing five of the parties' disputed terms. The court provided a written summary of its constructions a few days later.[1] The court now explains its reasoning below.

I. BACKGROUND

In this suit, Plaintiffs Acer, Inc., Acer America Corp., Gateway, Inc., HTC Corp., and HTC America, Inc.[2] seek a declaratory judgment that they do not infringe patents owned by Defendants Technology Properties, Patriot Scientific, and Alliacense (collectively "TPL"). All of the patents at issue relate to various aspects of microprocessors.

On November 30, 2012, the court held a claim construction hearing to consider five disputed terms. Prior to the case being reassigned to the undersigned, Judge Ware considered the same five terms.[3] He construed three of them and asked for more briefing on two of them, although he also provided a tentative construction for the two.[4]

The Eastern District of Texas also has considered related terms in another case that TPL filed in 2006 against unrelated third parties. In that case, Judge Ward held a claim construction hearing and issued a decision construing terms based upon patents with the same specification as the patents at issue in this suit.[5] Several terms he construed overlap with terms at issue here. Although the case resolved before proceeding to trial, TPL appealed a portion of the claim construction ruling to the Federal Circuit with respect to one of the three patents in suit; the Federal Circuit affirmed the district court's judgment against TPL.[6]

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[1] *See* Docket No. 381.

[2] Barco N.V. was originally a party and was a party to the motions at issue, but is no longer involved in the case.

[3] *See* Docket No. 336.

[4] *See id.*

[5] *See Tech. Properties Ltd. v. Matsushita Elec. Indus. Co., Ltd.*, 514 F. Supp. 2d 916, 927 (E.D. Tex. 2007) *aff'd sub nom.*, 276 F. App'x 1019 (Fed. Cir. 2008). At issue were United States Patent Nos. 5,809,336, 6,598,148, and 5,784,584.

[6] *See Tech. Properties Ltd., Inc. v. Arm, Ltd.*, 276 F. App'x 1019 (Fed. Cir. 2008).

The terms at issue are found in United States Patent No. 5,440,749 (the "'749 Patent") titled "High Performance, Low Cost Microprocessor Architecture,"[7] United States Patent No. 5,809,336 (the "'336 Patent") titled "High Performance Microprocessor Having Variable Speed System Clock,"[8] and United States Patent No. 5,530,890 (the "'890 Patent"), titled "High Performance, Low Cost Microprocessor."[9] All three patents derive from the same original patent application that was subject to a ten-way restriction requirement and eventually resulted in six different patents known as the Moore Microprocessor Portfolio patents, all of which share a common specification.

The '749 Patent claims an invention that accelerates the operation of microprocessors by fetching multiple instructions from memory per memory cycle. Because a CPU can execute instructions faster than it can fetch them from memory, fetching multiple instructions per memory cycle can improve overall performance.

The '336 Patent claims an invention that allows the frequency of a CPU to fluctuate based upon conditions. Traditional microprocessors use fixed frequency clocks to regulate the frequency with which the CPU operates. Fixed clocks generally have to be set lower than the CPU's maximum possible frequency to ensure proper operation under the worst-case conditions. The '336 Patent claims an invention that solves this problem by placing a ring oscillator on the same microchip as the CPU to act as the clock. Because the ring oscillator is on the same microchip and made out of the same components as the CPU, it is subject to the same environmental conditions and thus it will operate at a variable speed based upon conditions allowing the CPU to operate at higher rates during good conditions and lower rates during bad.

The '890 Patent relates to microprocessor architecture and claims a direct memory access mechanism. Most microprocessors have a direct memory access controller that handles the slow operation of reading and writing to memory so that the CPU can execute other instructions while waiting. The patent discloses a direct memory access CPU, which can execute some instructions in addition to reading and writing to memory for the CPU.

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[7] *See* Docket No. 358-2.

[8] *See* Docket No. 358-6.

[9] *See* Docket No. 368-2.

II. LEGAL STANDARDS

Claim construction is exclusively within the province of the court.[10] "To construe a claim term, the trial court must determine the meaning of any disputed words from the perspective of one of ordinary skill in the pertinent art at the time of filing."[11] This requires a careful review of the intrinsic record, comprised of the claim terms, written description, and prosecution history of the patent.[12] While claim terms "are generally given their ordinary and customary meaning," the claims themselves and the context in which the terms appear "provide substantial guidance as to the meaning of particular claim terms."[13] Indeed, a patent's specification "is always highly relevant to the claim construction analysis."[14] Claims "must be read in view of the specification, of which they are part."[15]

Although the patent's prosecution history "lacks the clarity of the specification and thus is less useful for claim construction purposes," it "can often inform the meaning of the claim language by demonstrating how the inventor understood the invention and whether the inventor limited the invention in the course of prosecution, making the claim scope narrower than it would otherwise be."[16] The court also has the discretion to consider extrinsic evidence, including dictionaries, scientific treatises, and testimony from experts and inventors. Such evidence, however, is "less significant than the intrinsic record in determining the legally operative meaning of claim language."[17]

Judge Ware has already considered all of the terms currently before the court. Although the court granted leave for parties to file motions for reconsideration, it will take as its starting point that

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[10] *See Markman v. Westview Instruments, Inc.*, 517 U.S. 370, 387 (1996).

[11] *Chamberlain Group, Inc. v. Lear Corp.*, 516 F.3d 1331, 1335 (Fed. Cir. 2008).

[12] *See id.*; *Phillips v. AWH Corp*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (internal citations omitted).

[13] *Phillips*, 415 F.3d at 1312, 1314.

[14] *Id.* at 1312-15.

[15] *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 979 (Fed. Cir. 1995) (en banc), *aff'd*, 517 U.S. 370 (1996); *see also Ultimax Cement Mfg. Corp v. CTS Cement Mfg. Corp.*, 587 F. 3d 1339, 1347 (Fed. Cir. 2009).

[16] *Phillips*, 415 F.3d at 1317 (internal quotations omitted).

[17] *Id.* (internal quotations omitted).

the earlier constructions are correct. Consistent with Local Rule 7-9, absent newly discovered material facts, change in law, or manifest failure to consider material facts or arguments, the court will not alter any earlier constructions.[18]

III. CLAIM CONSTRUCTION

A. "instruction register"

Plaintiffs' Proposed Construction	TPL's Proposed Construction
Register that receives and holds one or more instructions for supplying to circuits that interpret the instructions, in which any operands that are present must be right-justified in the register	Register that receives and holds one or more instructions for supplying to circuits that interpret the instructions

The parties dispute the construction of "instruction register" as used in claim 1 of the '749 Patent. The term "instruction register" was added to a wherein clause in claim 1 of the '749 patent during reexamination. The patent claims a microprocessor system

> wherein the microprocessor system comprises an instruction register configured to store the multiple sequential instructions and from which instructions are accessed and decoded.[19]

Judge Ware tentatively construed "instruction register" in the '749 patent as having its plain and ordinary meaning.[20] Quoting a dictionary, he determined that instruction register meant a "register in a central processing unit that holds the address of the next instruction to be executed."[21] After construing the term, the court noted that the prosecution history might convince the court to limit its construction and requested more briefing.[22]

The parties agree that the term has a slightly different meaning than the one the court previously adopted because the court's previous definition came from a software dictionary and the patents are hardware-related. The parties agree that the meaning of "instruction register" in the

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[18] *See Therasense, Inc. v. Becton, Dickinson & Co.*, 560 F. Supp. 2d 835, 844 (N.D. Cal. 2008) (following courts in the Northern District of California that "have required a litigant to meet the Civil Local Rule 7-9 standard when requesting reconsideration of a claim construction").

[19] *See* Docket No. 358-2, Reexam. Cert., col.1 ll.55-60.

[20] *See* Docket No. 336 at 11.

[21] *Id.* at 10 (quoting MICROSOFT COMPUTER DICTIONARY 276 (5th ed. 2002)).

[22] *See id.* at 11 n.23.

context of hardware is a "register that receives and holds one or more instructions for supplying to circuits that interpret the instructions." The court takes this construction as its starting point.

TPL urges the court to keep this construction while Plaintiffs argue for a more limited construction requiring that the operands in the register be right-justified. Even though Judge Ware's prior order indicated he was interested in an explanation of the prosecution history, the parties' arguments remain focused on the specification.

Plaintiffs argue that the specification requires the right-justified limitation for the register that it seeks. The Federal Circuit has instructed that "the specification may reveal a special definition given to a claim term by the patentee that differs from the meaning it would otherwise possess" or "reveal an intentional disclaimer."[23] However, only a clear disclaimer can justify narrowing the construction.[24] Where a patent consistently references a certain limitation or a preferred embodiment as the present invention, that also can serve to limit the scope of the invention where no other intrinsic evidence suggests otherwise.[25]

Here, Plaintiffs rely on a section of the patent specification that explains that the patented invention is able to use variable width operands because "operands must be right justified in the instruction register."[26] The specification describes this limitation as necessary to make the "magic" of the patent possible.[27] Plaintiffs argue that this is the equivalent of defining the "present invention," but the intrinsic evidence does not clearly support this limitation.

First, the right justified limitation is not a clear and consistent limitation given the overall context of the patent and the specification. The '749 patent is derived from an application that was subject to a ten-way restriction requirement that eventually resulted in six different patents. The original application, which eventually issued as the '749 patent disclosed all of the inventions in

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[23] *Phillips*, 415 F.3d at 1316.

[24] *See Voda v. Cordis Corp.*, 536 F.3d 1311, 1320 (Fed. Cir. 2008).

[25] *See Absolute Software, Inc.*, 659 F.3d at 1136.

[26] *See* Docket No. 358-2 at col.18 ll.43-45.

[27] *Id.*

what is now their extensive shared specification.[28] Plaintiffs rely on one small section of the common specification, with the heading "Variable Width Operands," covering about twenty lines of the thirty-three column specification.[29] Although this small section contains strong limiting language, because the specification is common to ten different inventions, it does not necessarily apply to the '749 Patent. In fact, Judge Ware previously held that one of those inventions, disclosed in the '584 patent, deals specifically with variable width operands.[30] But variable width operands are not essential to what is claimed in the '749 Patent. Claim 1 of the '749 Patent, the claim at issue here, does not contain the term operand or require variable width operands. Although parties focus on the '749 patent, the same reasoning applies to the '890 Patent.

Second, the specification actually discloses an embodiment where the operands are not right justified. In one embodiment, the instruction register receives four 8-bit instructions.[31] The specification disclosed two instructions, the "Read-Local-Variable XXXX" and "Write-Local-Variable XXXX," which are fixed width instructions that have a 4-bit opcode and a 4-bit operand.[32] These instructions can go into any of the four 8-bit slots in the instruction register and thus would contain operands that are not right justified.[33] At oral argument, Plaintiffs disputed TPL's characterization of these embodiments, arguing that the "4-bit operands" are not actually operands, but the location in temporary storage where the operand actually exists.[34] Even if the location in temporary storage is not a traditional operand, it acts similarly to one and adds further intrinsic evidence supporting a finding that the right justified limitation does not apply to the '749 and '890 patents.

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[28] *See generally*, Docket No. 358-2 at col.1-35.

[29] *See* Docket No. 358-2 at col.18 ll.35-56.

[30] *See* Docket No. 336 at 11.

[31] *See* Docket No. 358-2 at col.7 ll.50-58.

[32] *See* Docket No. 358-2 at col.31-32 ll.45-15.

[33] *See generally*, *id.* at col.7 ll.50-58.

[34] *See* Docket No. 382 at 106-07.

Plaintiffs do briefly cite to the prosecution history where, in a handwritten summary of an in-person interview in response to a Patent Office Action rejecting several of the claims of a related patent, the examiner stated "Claim 1: Operand width is variable + right adjusted."[35] Because various claims were withdrawn, however it is unclear to exactly what claim the examiner referred. This is not clear and unmistakable disavowal by the applicant.[36]

The parties agreed upon meaning alone should control. Accordingly, the court construes "instruction register" as the "register that receives and holds one or more instructions for supplying to circuits that interpret the instructions."

B. "ring oscillator"

Plaintiffs' Proposed Construction	TPL's Proposed Construction
an oscillator having a multiple, odd number of inversions arranged in a loop, wherein the oscillator is (1) non-controllable; and (2) variable based on the temperature, voltage and process parameters in the environment	an oscillator having a multiple, odd number of inversions arranged in a loop

The parties ask the court to construe the term "ring oscillator" as it is used in claim 1 of the '336 Patent. Judge Ware held that one of ordinary skill in the art would understand the term to mean "interconnected electronic components comprising multiple odd numbers of inverters arranged in a loop."[37] However, he ordered more briefing as to whether the court should give the terms a specialized meaning based upon the statements of the inventors during reexamination to distinguish their invention from the Talbot Patent.[38]

Once again, the parties agree on the basic meaning of the term, but dispute additional limitations. They agree that the meaning of the term is at least "an oscillator having a multiple, odd

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[35] Docket No. 363-19 at 2.

[36] *See Univ. of Pittsburgh of Commonwealth Sys. of Higher Educ. v. Hedrick*, 573 F.3d 1290, 1297 (Fed. Cir. 2009) (finding a "patentee may limit the meaning of a claim term by making a clear and unmistakable disavowal of scope during prosecution," but an examiner's summary of disavowal may only create a "weak inference" of the disavowal); *3M Innovative Properties Co. v. Avery Dennison Corp.*, 350 F.3d 1365, 1373 (Fed. Cir. 2003) (finding that prosecution history "cannot be used to limit the scope of a claim unless the *applicant* took a position before the PTO." (emphasis in the original)).

[37] Docket No. 336 at 13.

[38] *Id.* at 14-16.

number of inversions arranged in a loop." TPL urges the court to adopt meaning alone while the Plaintiffs argue that the term must be further limited to be: (1) non-controllable and (2) variable based on temperature, voltage, and process parameters in the environment. Plaintiffs argue that the prosecution history and specification support their position. As explained below, the prosecution history is too ambiguous to support Plaintiffs' construction in full, but the specification and especially the claim language do support Plaintiffs' second limitation.

1. Prosecution history

A "clear and unmistakable" disavowal by the patentee during prosecution or reexamination can narrow the scope of a claim.[39] However, because the "ongoing negotiations between the inventor and the examiner" can "often produce ambiguities," the doctrine only applies to "unambiguous disavowals."[40]

In the patent examiner's summary of his meeting with the patent owner, he wrote that

> the patent owner further argued that the reference of Talbot does not teach of a 'ring oscillator.' The patent owners discussed features of a ring oscillator, such as being non-controllable and being variable based upon the environment. The patent owner argued that these features distinguish over what Talbot teaches.[41]

The examiner finished his summary noting that he would "reconsider the current rejection based upon a forthcoming response, which will include arguments similar to what was discussed."[42] The subsequent written response argued that the Talbot reference did not teach a ring oscillator generally, and did *not* specifically argue that the ring oscillator was "non-controllable."[43] The examiner accepted this argument and withdrew the rejection.[44]

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[39] *Grober v. Mako Products, Inc.*, 686 F.3d 1335, 1341 (Fed. Cir. 2012), reh'g denied (Sept. 14, 2012).

[40] *Id.*

[41] Docket No. 357-5 at 5. The interview summary relates to the '148 patent, but it shares the same specification with the '336 patent.

[42] *Id.*

[43] *See id.*

[44] *Id.* at 27.

Plaintiffs argue that the examiner's summary is a clear disavowal that should limit the scope of the claim. The court disagrees. The Federal Circuit has suggested that where, as here, the "disavowal" is only an examiner's summary of a patentee's statement, it only creates a "weak inference" of a disavowal.[45] The subsequent prosecution history does not support Plaintiffs' claim construction because the patent owner appears to have made a different argument in his written reply, simply stating that the Talbot reference did not include a ring oscillator *generally* and not distinguishing the ring oscillator of the '336 Patent based on the examiner's stated exemplary features of ring oscillators.[46]

During prosecution, the patent owner also stated that the "the oscillator or variable speed clock varies in frequency but does not require manual or programmed inputs or external or extra components to do so."[47] This statement is not a disavowal because it only affirms that external inputs are "not required." The statement does not clearly impose a prohibition on all types of control.

2. Specification

Plaintiffs also argue that the specification supports their proposed construction. The specification describes the "ring oscillator" as having its frequency "determined by the parameters of temperature, voltage, and process."[48] Although this portion of the specification appears to disclose the preferred embodiment rather than constitute an express limitation on the claimed invention,[49] Claim 1 of the '336 Patent *claims* that the processing frequency of the CPU and the ring

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[45] *See Univ. of Pittsburgh*, 573 F.3d at 1297.

[46] *See generally, Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1124 (Fed. Cir. 2004) (describing a series of exchanges between the patent owner and the examiner as the parties "talking past one another" and finding no clear evidence of a disavowal from the confused exchange).

[47] Docket No. 363-4 at 6.

[48] *See* Docket No. 358-6 at col.16 ll.59-60.

[49] *See Brookhill-Wilk 1, LLC. v. Intuitive Surgical, Inc.*, 334 F.3d 1294, 1301-02 (Fed. Cir. 2003) ("statements from the description of the preferred embodiment are simply that-descriptions of a preferred embodiment. . . Absent a clear disclaimer of particular subject matter, the fact that the inventor anticipated that the invention may be used in a particular manner does not limit the scope to that narrow context.")

oscillator vary together due to manufacturing variations, operating voltage, and temperature.[50] The claim itself provides that the "ring oscillator" is "constructed of the same process technology with corresponding manufacturing variations" on the same single integrated circuit so that its performance will fluctuate with the CPU because they are subject to the same "manufacturing variations" and "operating voltage and temperature."[51] During oral argument, TPL admitted that a ring oscillator on the same microprocessor as the CPU will vary based upon voltage, temperature, and process variations.[52] Therefore, based upon the claim language and the specification, the court finds that the disclosed "ring oscillator" varies with voltage, temperature, and process variations.

Even though the claimed "ring oscillator" is "determined by the parameters of temperature, voltage, and process," it does not necessarily follow, as Plaintiffs' argue, that the "ring oscillator" must be non-controllable.[53] The claims do not mention "controllable" or "non-controllable" in relation to the "ring oscillator" and neither does the specification. The term "non-controllable" is only used by the patent examiner in the prosecution history discussed above. Additionally, in the preferred embodiment, the "ring oscillator" is "determined" by temperature, voltage, and process,[54] which suggests at least one embodiment in which the ring oscillator is controlled.

Because of the clear limitation in the claims that temperature, voltage, and process determine the "ring oscillator's" frequency, the court includes those limitations in the construction of the term, but does not find similar support for importing the "non-controllable" limitation. The court therefore construes "ring oscillator" as "an oscillator having a multiple, odd number of inversions arranged in a loop, wherein the oscillator is variable based on the temperature, voltage and process parameters in the environment."

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[50] *See* Docket No. 358-6, Reexam. Cert. col.2 ll.3-5.

[51] *Id.* at col.1-2 ll.59-05.

[52] *See* Docket No. 382 at 49:3-7.

[53] *See, e.g., Brookhill-Wilk*, 334 F.3d at 1301-02.

[54] *See* Docket No. 358-6 at col.16 ll.59-60.

C. "separate DMA CPU"

Plaintiffs' Proposed Construction	TPL's Proposed Construction
a central processing unit that accesses memory and that fetches and executes instructions directly, separately, and independently of the main central processing unit	Electrical circuit for reading and writing to memory that is separate from a main CPU

Judge Ware previously construed the term "separate direct memory access central processing unit" ("separate DMA CPU") from Claim 11 of the '890 Patent. Claim 11 claims

> A microprocessor, which comprises a main central processing unit and a separate direct memory access [DMA] central processing unit [CPU] in a single integrated circuit comprising said microprocessor . . .

The court construed "separate DMA CPU," consistent with its plain and ordinary meaning as "a central processing unit that accesses memory and that fetches and executes instructions directly, separately, and independently of the main central processing unit."[55] Plaintiffs urge the court to keep this construction while TPL argues that previously unaddressed parts of the prosecution history support a different construction broad enough to include standard DMA controllers, which do not execute instructions.

TPL's primary argument is that the history of the Moore patents supports a broader construction. TPL argues that the DMA CPU that fetches and executes its own instructions was one of the ten categories of inventions derived from the original application, but not the invention that eventually became the patent at issue, the '890 Patent. As explained above, the original patent application for what became the '749 Patent was subject to a ten-way restriction. A restriction indicates that "two or more independent and distinct inventions are claimed in one application."[56] One of these 10 categories of inventions was focused on a "microprocessor system having a DMA for fetching instruction[s] for a CPU and itself."[57] The patentee eventually abandoned this application. The '890 Patent came from a different category of invention "drawn to a microprocessor architecture."[58] TPL argues that because the '890 Patent came from a different

[55] Docket No. 336 at 13.

[56] 35 U.S.C. § 121.

[57] Docket No. 368-7 at 3.

[58] *Id*. *See also* Docket No. 356 at 3-4.

invention category, it should not be read to include the definition of the "DMA CPU" that was the subject of another invention.

The court disagrees. The fact that one abandoned patent focused on a particular subject matter does not necessarily mean that same subject matter cannot be within the scope of another related patent based upon the same specification. First, restriction requirements have little, if any, evidentiary weight.[59] Second, there is nothing in the claims to suggest that "DMA CPU" should have anything other than its plain and ordinary meaning. Third, the specification supports the plain and ordinary meaning. The specification discloses a "DMA CPU" in figures 2 and 9. When describing figure 2, the specification states that the "DMA CPU 72 controls itself and has the ability to fetch and execute instructions. It operates as a co-processor to the main CPU 70."[60] The "DMA CPU 314" in figure 9 is part of another microprocessor that the specification describes as equivalent to the microprocessor in figure 2.[61] A separate passage in a later section of the specification describes another embodiment where the "DMA processor 72 of the microprocessor 50 has been replaced with a more traditional DMA controller 314."[62] The specification goes on to describe the characteristics of a DMA controller. These sections are clear that a DMA controller is distinct from a DMA CPU and the patent refers to each by name where appropriate. Thus where the patent claims a DMA CPU, it means a DMA CPU and not a DMA controller.

TPL also argues that statements made during reexamination by the requester and the examiner support its position. The court disagrees. First, the examiner and the reexamination requester made the cited statements, not the patent owner.[63] Second, regardless of who made the

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[59] *See Honeywell Int'l, Inc. v. ITT Indus., Inc.*, 452 F.3d 1312, 1319 (Fed. Cir. 2006); *Rambus Inc. v. Hynix Semiconductor Inc.*, 569 F. Supp. 2d 946, 962 (N.D. Cal. 2008) ("In laying out the details of the original restriction requirement, the court recognizes its limited evidentiary significance.").

[60] *See* Docket No. 368-2 at col.8 ll.22-24.

[61] *See id.* at col.9 ll.5-6.

[62] *Id.* at col.12 ll.62-65.

[63] *See 3M Innovative Properties Co.*, 350 F.3d at 1373 (finding that prosecution history "cannot be used to limit the scope of a claim unless the *applicant* took a position before the PTO."(emphasis in the original)).

statements, they do not clearly show that the term "DMA CPU" was understood to include a DMA controller.[64]

During oral argument, TPL argued that the term "independently" in the original construction is unsupported.[65] The court agrees with this point. Even if the DMA CPU fetches and executes its own instructions, it cannot do so independently. The reason for putting the CPU and DMA CPU on the same chip is so they can work together.[66] Otherwise, the evidence in support of changing the court's prior construction is unpersuasive.

The court construes "separate DMA CPU" as "a central processing unit that accesses memory and that fetches and executes instructions directly and separately of the main central processing unit."

D. "supply the multiple sequential instructions"

Plaintiffs' Proposed Construction	TPL's Proposed Construction
provide the multiple sequential instructions in parallel (as opposed to one-by-one) to said central processing unit integrated circuit during a single memory cycle without using a prefetch buffer or a one-instruction-wide instruction buffer that supplies on instruction at a time	provide the multiple sequential instructions in parallel to said central processing unit integrated circuit during a single memory cycle

The parties ask the court to construe the phrase "supply the multiple sequential instructions to said central processing unit integrated circuit during a single memory cycle," from claim 1 of the '749 patent. Judge Ware previously determined that this phrase was composed of commonly used words that the patentee intended to have their plain and ordinary meaning. Plaintiffs argue for a narrower construction based upon disavowals during reexamination while TPL argues for a broad construction. The parties specifically dispute what limitations the patent places on how the "multiple sequential instructions" are provided to the CPU.

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[64] *See id.* at 1346-47 ("An applicant's silence in response to an examiner's characterization of a claim does not reflect the applicant's clear and unmistakable acquiescence to that characterization if the claim is eventually allowed on grounds unrelated to the examiner's unrebutted characterization.").

[65] *See* Docket No. 382 at 121-22.

[66] *See* Docket No. 368-2, Reexam. Cert., col.1 ll.22-24; Docket No. 368-2 at col.8 ll.22-24 (the DMA CPU "operates as a co-processor to the main CPU").

During reexamination, TPL unambiguously disavowed that instructions could be provided to the CPU one-by-one. The PTO issued a reexamination rejecting claims in the '749 Patent, including claim 1, based upon the "Edwards" patent[67] and an article by Doug MacGregor.[68] To distinguish the Edwards patent, TPL argued that in the Edwards patent, "instructions are supplied to a one-instruction-wide instruction buffer, one at a time," while for the '749 Patent "[f]etching multiple instructions into a prefetch buffer and then supplying them one at a time is not sufficient to meet the claim limitation—the supplying of 'multiple sequential instructions to a CPU during a single memory cycle.'"[69] Similarly, in distinguishing the invention in MacGregor, TPL wrote that "non-parallel supplying of instructions to the CPU is not supplying them to the CPU during a single memory cycle as required by the claim."[70] By this language, TPL clearly and unambiguously disavowed supplying instructions to the CPU one-by-one.

Plaintiffs also urge the court to find TPL disavowed specific structures or components in the above statements, but these statements as to structures are not clearly disavowals because they are made in the context of describing the prior art. There may be ways of incorporating such structures consistent with not supplying the instructions one-by-one.

Accordingly, the court construes the phrase "supply the multiple sequential instructions to said central processing unit integrated circuit during a single memory cycle" as "provide the multiple sequential instructions in parallel (as opposed to one-by-one) to said central processing unit integrated circuit during a single memory cycle."

E. "clocking said CPU"

Plaintiffs' Proposed Construction	TPL's Proposed Construction
timing the operation of the CPU such that it will always execute at the maximum frequency possible, but never too fast	timing the operation of the CPU

[67] U.S. Patent No. 4,680,698.

[68] Doug MacGregor *et al.*, "The Motorola MC68020," IEEE Micro 101 (August 1984).

[69] Docket No. 358-3 at 27.

[70] *Id.* at 46.

The parties ask the court to construe "clocking said CPU," which appears in claims 1, 6, and 10 of the '336 Patent. Generally speaking, "clocking the CPU" refers to using the system clock to control the speed of the CPU. Judge Ware previously considered "clocking said CPU" and based upon the plain and ordinary meaning of the term, construed it as "providing a timing signal to said central processing unit." The court considered other language in the written description that suggested a more limited construction, but ultimately determined that the patentee had not "demonstrated a clear intention to limit the claim scope."[71] Similarly, Judge Ward construed a longer term[72] from claim 1 containing the term "clocking said CPU" as "an oscillator that generates the signal(s) used for timing the operation of the CPU."[73] In construing the term, Judge Ward similarly did not adopt the type of limiting language that Plaintiffs advocate.

As discussed above and explained in the patent, the disclosed invention uses a variable speed clock—a ring oscillator—that varies with temperature, voltage, and process. The specification states that "[b]y deriving system time from the ring oscillator 430, CPU 70 will always execute at the maximum frequency possible, but never too fast."[74] Plaintiffs argue that this is a clear limitation that should be read into the claims. In general, absent a clear intention to limit the scope of a claim, a description of an embodiment should not limit claim language that otherwise has a broader effect.[75] This rule applies even if the patent only describes a single embodiment.[76] Judge Ware previously considered and rejected Plaintiffs attempt to limit the claim based upon the specification and this court agrees. There is no support in the claim language itself for the requirement that the clock always forces the CPU to operate at its maximum frequency. The court finds that operating at

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[71] Docket No. 336 at 17-18 (quoting *Innova/Pure Water*, 381 F.3d at 1117).

[72] Judge Ward construed "an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit."

[73] *Tech. Properties Ltd. v. Matsushita Elec. Indus. Co., Ltd.*, 514 F. Supp. 2d 916, 927 (E.D. Tex. 2007) aff'd sub nom., 276 F. App'x 1019 (Fed. Cir. 2008).

[74] *See* Docket No. 358-6 at col.16-17 ll.63-2.

[75] *See Innova/Pure Water*, 381 F.3d at 1117.

[76] *See id.*

the maximum frequency is merely the preferred embodiment and not the only manner in which the invention can operate.

Plaintiffs also try to introduce evidence from the prosecution history to support their argument. Although Plaintiffs quote a section from the prosecution history where the applicants used the magic words "the present invention," what the applicants disclosed is that the present invention includes a variable speed clock on the same microprocessor as the CPU and thus its speed will vary based upon environmental conditions.[77] This is exactly what is claimed in claim 1. The excerpt goes on to explain that one advantage of the variable speed clock is that it "allows the microprocessor to operate at its fastest safe operating speed,"[78] but again, this is just one embodiment and not necessarily a *requirement* of the invention. Plaintiffs' other citations to the prosecution history are similarly unconvincing.

Because the parties have not convinced the court that the prior construction was in error, the Court declines to change its construction. Accordingly, the court construes "clocking said CPU" as "providing a timing signal to said central processing unit."

IV. CONCLUSION

For the reasons set forth above, the court construes the claims as follows:

CLAIM TERM	CONSTRUCTION
"instruction register"	Register that receives and holds one or more instructions for supplying to circuits that interpret the instructions
"ring oscillator"	an oscillator having a multiple, odd number of inversions arranged in a loop, wherein the oscillator is variable based on the temperature, voltage and process parameters in the environment
"separate DMA CPU"	a central processing unit that accesses memory and that fetches and executes instructions directly and separately of the main central processing unit
"supply the multiple sequential instructions to said central processing unit integrated circuit during a single memory cycle"	provide the multiple sequential instructions in parallel (as opposed to one-by-one) to said central processing unit integrated circuit during

[77] *See* Docket No. 358-9 at 4-5.

[78] *Id.* at 5.

	a single memory cycle
"clocking said CPU"	Providing a timing signal to said central processing unit

Dated: August 21, 2013

PAUL S. GREWAL
United States Magistrate Judge